providing a semiconductor substrate having a first region where a first oxide layer thickness is desired and a second region where a second oxide layer thickness is desired, wherein said first oxide layer thickness is greater than said second oxide layer thickness;

introducing halogen-containing impurities into an exposed surface of said semiconductor substrate to form a higher halogen concentration in said first region than in said second region;

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region; and

forming a first memory gate electrode on said second oxide layer thickness, said second oxide layer thickness formed on said semiconductor substrate in a memory region.

4. (As previously amended) The method of claim 2 wherein introducing said halogen-containing impurities comprises an ion implantation.

5. (As previously amended) The method of claim 2 wherein introducing said halogen-containing impurities comprises introducing halogen-containing impurities into said first region and wherein said second region has substantially no halogen concentration therein.

6. (Five times amended herein) A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first semiconductor surface where a first oxide layer thickness is desired and a second semiconductor surface where a second oxide layer thickness is desired, wherein said first semiconductor surface is adjacent said second semiconductor surface;

introducing halogen-containing impurities into said semiconductor substrate to form a higher halogen concentration in said semiconductor substrate substantially below said first semiconductor surface than in said semiconductor substrate substantially below said second semiconductor surface;

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness disposed above said first semiconductor surface and said second oxide layer thickness disposed above said second semiconductor surface; and

wherein introducing said halogen-containing impurities comprises introducing halogen-containing impurities into said semiconductor substrate substantially below said first semiconductor surface at a first concentration and introducing halogen-containing impurities into said semiconductor substrate substantially below said second semiconductor surface at a second concentration, said first concentration greater than said second concentration, both said first and second concentrations formed of a dosage of said halogen-containing impurities greater than about 1 x 10^{14} carriers/cm^2 and less than about 1 x 10^{15} carriers/cm^2.

7. (As previously amended) The method of claim 6 wherein said halogen-containing impurities promote oxide growth on said semiconductor substrate such that said first oxide layer thickness is greater than said second oxide layer thickness.

8. (As previously amended) The method of claim 2 wherein said halogen-containing impurities are selected from fluorine bearing impurities, chlorine bearing impurities, bromine bearing impurities, and iodine bearing impurities.

9. (As previously amended) The method of claim 2 wherein said semiconductor substrate also includes a third region where a third oxide layer thickness is desired, and wherein introducing said halogen-containing impurities also introduces halogen-containing impurities such that a different halogen concentration is formed in said third region than in said first region and in said second region.

10. (As previously amended) The method of claim 2 wherein said semiconductor device comprises a flash EEPROM semiconductor device.

11. (As filed) The method of claim 2 wherein said first memory gate electrode comprises a floating gate electrode.

12. (As filed) The method of claim 11 wherein said first memory gate electrode is part of a stack gate cell.

13. (As filed) The method of claim 11 wherein said first memory gate electrode i part of a split gate cell.

14. (As filed) The method of claim 2 wherein said first memory gate electrode comprises a control gate electrode.

15. (As filed) The method of claim 14 wherein said first memory gate electrode is part of a stack gate cell.

16. (As filed) The method of claim 14 wherein said first memory gate electrode is part of a split gate cell.

20. (Four times amended herein) A method of forming a semiconductor integrated circuit, said method comprising:

providing a semiconductor substrate, said semiconductor substrate comprising a memory cell region, a first region for a MOS transistor, and a second region for a high voltage device;

forming a gate dielectric layer comprising an oxide overlying said semiconductor substrate including said first region and said second region;

selectively implanting halogen-containing impurities through said gate dielectric layer and into said second region; and

simultaneously forming a first thickness of dielectric material overlying said first region and forming a second thickness of dielectric material overlying said second region by an oxidizing process, wherein said halogen-containing impurities in said second region promote formation of said second thickness of dielectric material.

21. (Three times amended herein) The method of claim 20

wherein said selectively implanting halogen-containing impurities into said first region also includes selectively implanting halogen-containing impurities into said second region such that said first region has a greater halogen concentration than said second region, said halogen-containing impurities in said second region formed of a dosage greater than about 1×10^{14} carriers/cm^2 and less than about 1×10^{15} carriers/cm^2

22. (As filed) The method of claim 20 wherein said halogen-containing impurities are selected from fluorine bearing impurities, chlorine bearing impurities, bromine bearing impurities, and iodine bearing impurities.

23. (As filed) The method of claim 20 further comprising forming a third thickness of dielectric material overlying a third region, said third region being spatially apart from said first region and said second region.

24. (Twice amended herein) A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first semiconductor surface area where a first oxide layer thickness is desired and a second semiconductor surface area where a second oxide layer thickness is desired, said first semiconductor surface area directly adjacent said second semiconductor surface area;

forming a dielectric layer on said substrate;

masking said dielectric layer to expose said first semiconductor surface area;

introducing halogen-containing impurities through said dielectric layer and into said semiconductor substrate to form a higher halogen concentration in a volume of said semiconductor substrate substantially below said first semiconductor surface area than in a volume of said semiconductor substrate substantially below said second semiconductor surface area; and

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first semiconductor surface area and said second oxide layer thickness at said second semiconductor surface area;

said oxidizing process comprising a thermal anneal at about 780 to about 1000 degrees Celsius, and for a duration of about ten (10) minutes to about five (5) hours.

25. (As previously added) The method of claim 24 wherein said halogen-containing impurities promote oxide growth on said semiconductor substrate such that said first oxide layer thickness is greater than said second oxide layer thickness.

26. (As previously added) The method of claim 24 wherein said halogen-containing impurities are selected from fluorine bearing impurities, chlorine bearing impurities, bromine bearing impurities, and iodine bearing impurities.

27. (Four times amended herein) A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first semiconductor surface area where a first oxide layer thickness is desired, a second semiconductor surface area where a second oxide layer thickness is desired, and a third semiconductor surface area where a third oxide layer thickness is desired, wherein said first and second semiconductor surface areas are contiguous;

introducing a halogen-containing impurities into said semiconductor substrate to form a higher halogen concentration in a first volume of said semiconductor substrate substantially below said first semiconductor surface area than in a second volume of said semiconductor substrate substantially below said second semiconductor surface area, and a different halogen concentration in a third volume of said semiconductor substrate substantially below said third semiconductor surface area than in said first volume and said second volume, each of said higher halogen concentration and said different halogen concentration; and

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first semiconductor surface area and said second oxide layer thickness at said second semiconductor surface area.

28. (Amended once herein) The method of claim 27 wherein said performing an oxidizing process also simultaneously forms said third oxide layer thickness at said third semiconductor surface area.

29. (Previously once amended) The method of claim 6 wherein at least one of said first and second concentrations formed of a dosage of said halogen-containing impurities greater than about 1×10^{14} carriers/cm^2 and less than about 1×10^{15} carriers/cm^2.

30. (As previously added)The method of claim 20 wherein said forming said first and second thickness of dielectric material comprises an anneal process performed at about 780 to about 1000 degrees Celsius, and for a duration of about ten (10) minutes to about five (5) hours.

31. (As previously added) The method of claim 30 wherein said anneal process is further performed at a pressure of about 760 Torr.

32. (Once amended herein) A method of forming a semiconductor device, the method comprising:

providing a substrate having a first region and a second region;

introducing halogen-containing impurities into the substrate to form a higher concentration in the first region than in the second region;

placing the substrate in an oxidizing environment, wherein a thicker oxide layer forms over the first region where the halogen-containing impurities are located than over the second region;

in a single step, forming a conductive layer disposed above the first region and the second region; and

removing portions of the oxide layer and the conductive layer to form gate structures disposed over the substrate.

REMARKS

Claims 2, 4-16 and 20-32 were pending in this application. Claims 2, 6, 20, 24, 24, 27, 28 and 32 have been amended. Hence, claims 2, 4-16 and 20-32 are now pending. Reconsideration of the subject application as amended is respectfully requested.

Claims 2, 4, 5, 8, 9 and 32 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Grider et al.

Claim 10 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Grider et al. as applied to claims 2, 4, 5, 8, 9 and 32 above.

Claims 11-16 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Grider et al. as applied to claims 2, 4, 5, 8, 9 and 32 above.

Claims 6, 7 and 20-31 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Grider et al. as applied to claims 2, 4, 5, 8, 9 and 32 above.

REJECTIONS UNDER 35 U.S.C. §§ 102 and 103

Claims 2, 4, 5, 8, 9 and 32 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Grider et al. (U.S. Patent No. 6,093,659). Claims 10-16 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Grider et al. as applied to claims 2, 4, 5, 8, 9 and 32 above. Claims 6, 7 and 20-31 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Grider et al. as applied to claims 2, 4, 5, 8, 9 and 32 above. Applicant respectfully traverses the rejections with respect to independent claims 2, 6, 20, 24, 27 and 32.